CLAIMS

1. A test circuit comprising:

a first transistor pair including a first transistor and a second transistor coupled with a device under test; and

a second transistor pair including a third transistor and a fourth transistor coupled with a dummy device, the first transistor and the third transistor having a first common gate connection configured to be driven by a first variable voltage, the first transistor and the third transistor being biased by a first variable bias voltage, the second transistor and the fourth transistor having a second common gate connection configured to be driven by a second variable voltage, the second transistor and the fourth transistor being biased by a second variable bias voltage.

2. The test circuit of claim 1 wherein the first transistor and the third transistor each comprise a p-channel transistor and the second transistor and the fourth transistor each comprise a p-channel transistor.

3. The test circuit of claim 2 wherein:

the first transistor has a drain coupled to the device under test; and

the second transistor has a source coupled to the device under test.

4. The test circuit of claim 3 wherein:

the third transistor has a drain coupled to the dummy device; and

the fourth transistor has a source coupled to the dummy device.

5. The test circuit of claim 4 where the first transistor, the second transistor, the third transistor and the fourth transistor are formed in an n-well on a p-substrate.

6. The test circuit of claim 5 wherein the first transistor is substantially matched to the third transistor and the second transistor is substantially matched to the fourth transistor.

7. The test circuit of claim 1 further comprising

a driver circuit coupled to the first common gate connection and the second common gate connection; and

a bias circuit having one output coupled to the first transistor and the third transistor for providing the first bias voltage and another output coupled to the second transistor and the fourth transistor for providing the second bias voltage.

8. The test circuit of claim 7 wherein the transistors, the driver circuit and the bias circuit are integrated on a common semiconductor substrate.

9. The test circuit of claim 7 wherein the transistors and the device under test are integrated on a common semiconductor substrate.

10. The test circuit of claim 9 wherein the driver circuit and the bias circuit are further integrated on the common semiconductor substrate.

11. The test circuit of claim 1 further comprising a clock signal generating circuit coupled with the first common gate connection and the second common gate connection and configured to generate the first variable voltage and the second variable voltage.

12. The test circuit of claim 11 wherein the clock signal generating circuit comprises:

an oscillator; and

a frequency division circuit for reducing frequency of signals generated by the oscillator to provide for allowing monitoring frequencies of the first variable voltage and the second variable voltage.

13. The test circuit of claim 12 wherein the frequency division circuit comprises one or more counters.

14. The test circuit of claim 11 wherein the clock signal generating circuit comprises one or more voltage controlled oscillators.

15. The test circuit of claim 14 wherein the clock signal generating circuit further comprises circuitry to control frequency division of the signals generated by the oscillator.

16. The test circuit of claim 1 further comprising:

a digital to analog converter coupled to the first transistor pair and the second transistor pair.

17. The test circuit of claim 16 wherein the digital to analog converter controls amplitudes of one or more of the first variable voltage, first variable bias voltage, the second variable voltage, and the second variable bias voltage.

18. The test circuit of claim 17 wherein the digital to analog converter comprises a digital input configured to receive an external digital control signal.

19. The test circuit of claim 1 wherein the device under test and the dummy device comprise multiple electrode capacitances.

20. The test circuit of claim 19 further comprising a field continuation structure located proximate to the device under test.

21. The test circuit of claim 20 further comprising a field continuation structure located proximate to the dummy device.

22. The test circuit of claim 19 wherein the device under test comprises an active semiconductor device.

23. The test circuit of claim 22 wherein the device under test comprises a field effect transistor.

24. The test circuit of claim 23 wherein the device under test comprises a field effect transistor for characterization of capacitances between a gate electrode, a source electrode, a drain electrode, a well electrode and a body electrode of the field effect transistor.

25. The test circuit of claim 24 wherein the device under test comprises a field effect transistor formed in the substrate of a semiconductor containing the test circuit.

26. The test circuit of claim 24 wherein the device under test comprises a field effect transistor formed in a diffused well formed in the substrate of a semiconductor containing the test circuit.

27. The test circuit of claim 24 wherein the device under test comprises a field effect transistor formed on an insulating substrate.

28. The test circuit of claim 22 wherein the device under test comprises a field effect transistor floating gate memory transistor.

29. The test circuit of claim 22 wherein the device under test comprises one field effect transistor of a plurality of a field effect transistors, each field effect transistor having one transistor width of a range of transistor widths and one transistor length of a range of transistor lengths to isolate capacitive contributions of width and length dependent components of device capacitance.

30. A characterization method for a device under test, the method comprising:

applying a bias voltage to a test circuit including a first transistor coupled to the device under test, a second transistor coupled to a dummy device, a third transistor coupled to the device under test and the first transistor and a fourth transistor coupled to the dummy device and the second transistor, the transistors being of a common type;

applying non-overlapping clocking signals to transistors of the test circuit to produce test signals for application to the device under test;

detecting a current in one or more transistors from the device under test; and

varying the bias voltage.

31. The characterization method of claim 30 wherein varying the bias voltage comprises:

varying the bias voltage from a first value to a second value; and

detecting the current at a plurality of bias voltage values.

32. The characterization method of claim 30 wherein varying the bias voltage comprises:

applying one or more positive bias voltages; and

applying one or more negative bias voltages.

33. The characterization method of claim 30 further comprising:

subtracting parasitic capacitances associated with the dummy device from parasitic capacitances associated with the device under test to determine a capacitance of interest of the device under test.

34. The characterization method of claim 30 further comprising:

applying a first bias voltage to the third transistor and measuring current in the third transistor;

applying the first bias voltage to the first transistor and measuring current in the first transistor; and

determining capacitance associated with the device under test from the difference between the current in the third transistor and the current in the first transistor.

35. The characterization method of claim 30 wherein the device under test comprises a first capacitor and the dummy device comprises a second capacitor.

36. The characterization method of claim 35 wherein an area component of capacitance of the first capacitor substantially matches an area component of capacitance of the second capacitor.

37. The characterization method of claim 35 wherein a perimeter component of capacitance of the first capacitor substantially matches a perimeter component of capacitance of the second capacitor.

38. The test circuit of claim 35 further comprising a field continuation structure located proximate to the device under test.

39. The test circuit of claim 35 further comprising a field continuation structure located proximate to the dummy device.

40. The test circuit of claim 35 wherein the device under test further comprises a multiple electrode capacitance.

41. The test circuit of claim 35 wherein the dummy device further comprises a multiple electrode capacitance.

42. The characterization method of claim 30 wherein the device under test comprises an interconnect capacitance.

43. The characterization method of claim 42 wherein the device under test comprises a multiple-finger segment of interconnect material.

44. The characterization method of claim 42 wherein the device under test comprises a single-line segment of interconnect material.

45. The characterization method of claim 42 wherein the device under test comprises a layer to layer capacitance in a semiconductor device.

46. The characterization method of claim 45 wherein the device under test comprises two crossing segments of interconnect material on different layers.

47. The characterization method of claim 42 wherein the device under test comprises two substantially parallel segments of interconnect material.

48. The characterization method of claim 42 wherein the device under test comprises a capacitance between interconnect segments each on a same layer of material in a semiconductor device.

49. The characterization method of claim 42 wherein the device under test comprises a capacitance between a segment of interconnect material and a substrate of a semiconductor device.

50. The characterization method of claim 30 wherein the device under test comprises one or more layers of the semiconductor in which the test circuit is formed for characterizing a manufacturing process related parameter.

51. The characterization method of claim 50 wherein the manufacturing process related parameter is one of doping profile, insulator thickness and dielectric properties.

52. The characterization method of claim 50 wherein the manufacturing process related parameter is frequency dependency of a capacitance.

53. The characterization method of claim 52 wherein the manufacturing process related parameter is frequency dependency of a metal oxide semiconductor (MOS) capacitor inversion layer.

54. The characterization method of claim 53 wherein the manufacturing process related parameter is carrier generation rate in a MOS capacitor inversion layer.

55. The characterization method of claim 53 wherein the manufacturing process related parameter is one of trap density, impurity and defect densities in the one or more layers of the semiconductor.

56. The characterization methods of claim 55 wherein the device under test forms part of a semiconductor memory array.

57. The characterization method of claim 52 wherein the manufacturing process related parameter is location of trapped charge in a gate dielectric of a transistor.

58. The characterization method of claim 30 wherein the manufacturing process related parameters comprise location and density of trapped charge in a gate dielectric of a transistor.

59. The characterization methods of claim 58 wherein the device under test forms part of a semiconductor memory array.

60. A method for testing a device under test on a semiconductor substrate, the method comprising:

applying a bias voltage to a test circuit, the test circuit including first and second transistors coupled to the device under test and third and fourth transistors coupled to a dummy device selected to match portions of

the device under test, the test circuit formed on the semiconductor substrate;

applying a first test signal to the first transistor and a second test signal to the second transistor to selectively apply a current to the device under test;

detecting the current in the device under test in response to the test signals;

applying the first test signal to the third transistor and the second test signal to the fourth transistor to selectively apply current to the dummy device;

detecting the current in the dummy device in response to the test signals; and

determining a capacitance of a portion of the device under test using the current in the dummy device and the current in the device under test.

61. The method of claim 60 further comprising:

varying the bias voltage across a voltage range defined by a minimum voltage and a maximum voltage.

62. The method of claim 60 wherein applying the bias voltage comprise:

applying the bias voltage to a first terminal of the device under test, the device under test having a second terminal at a voltage biasing the semiconductor substrate.

63. The method of claim 60 wherein one or both of the minimum voltage and the maximum voltage are less than the voltage associated with the substrate.

64. The method of claim 60 wherein applying the test signals comprise:

applying a first phase of the first test signal to produce a first current in the device under test; and

applying a complementary second phase of the second test signal to produce a second current in the device under test.

65. The method of claim 64 wherein applying the test signals further comprise:

applying the first phase of the first test signal to produce a third current in the dummy device; and

applying the complementary second phase of the second test signal to produce a fourth current in the dummy device.

66. The method of claim 60 further comprising:

applying selection signals to select the test circuit and the device under test among a plurality of similar test circuits associated with other devices under test.

67. The method of claim 66 further comprising:

generating the selection signals at on-chip circuitry formed on the semiconductor substrate.

68. The method of claim 60 wherein applying the test signal comprises:

applying one of a sinusoidal voltage, a triangle voltage and a variable amplitude voltage.

69. The method of claim 60 further comprising:

selecting a peak to peak amplitude of the test signal voltage to compensate capacitive perturbations in the circuit to minimize measurement error.

70. The method of claim 60 further comprising:

substituting a known capacitive value for the device under test; and

identifying optimum wave forms for the test signal voltage measuring the known capacitive value.

71. The method of claim 60 further comprising:

applying a source voltage and a drain voltage to both of an independent test transistor and a sense transistor having a gate coupled to an internal node of the test circuit;

measuring currents in the independent test transistor and the sense transistor; and

varying gate voltage of the independent test transistor until the current in the independent test transistor matches the current in the sense transistor.

72. The method of claim 60 further comprising:

selecting the dummy device having parasitic parameters which cancel parasitic parameters of the device under test when determining the capacitance of the device under test.

73. Apparatus for measuring electrical parameters comprising:

an array of test circuits, each test circuit driven by a respective clock up signal, a respective clock down signal, a first Vhigh signal, a second Vhigh signal and a Vlow signal, each test circuit associated with a device under test and a dummy device; and

a multiplexing circuit for coupling a limited number of control pads to respective test circuits of the array of test circuits for unique selection of a test circuit to be interrogated for measuring electrical parameters of the device under test of the test circuit to be interrogated.

74. The apparatus of claim 73 wherein the multiplexing circuit comprises:

a circuit configured to select the test circuit to be interrogated by asserting at least one of its associated clock up signal and clock down signal while maintaining other test circuits in the array in a non-selected mode.

75. The apparatus of claim 74 wherein the multiplexing circuit comprises:

a clock off node associated with a control pad biasable to a predetermined voltage level to disable switches of the test circuits of the array of test circuits; and

a plurality of high impedance elements substantially isolating the clock off node from common switch nodes, the common switch nodes shared by a common group of test circuits of the array of test circuits.

76. The apparatus of claim 75 wherein the high impedance elements comprise one or more transistors.

77. The apparatus of claim 74 wherein the multiplexing circuit comprises:

isolation transistors positioned in series with one or more test circuits for electrically coupling the test circuit to be interrogated with a control pad.

78. The apparatus of claim 77 further comprising:

biasing elements coupled with the isolation transistors to turn off the isolation transistors when the isolation transistors are not accessed.

79. The apparatus of claim 78 further comprising:

a common isolation transistor shut-off pad coupled to each of the biasing elements.

80. The apparatus of claim 73 wherein the array of test circuits and the multiplexing circuits are integrated in a common semiconductor device.

81. The apparatus of claim 80 further comprising:

a control circuit for generating control signals to control the multiplexing circuit.

82. The apparatus of claim 81 wherein the control circuit is integrated in the common semiconductor device.

83. The apparatus of claim 73 wherein two or more test circuits of the array of test circuits are coupled with respective field effect transistors for measuring electrical parameters of each field effect transistor.

84. The apparatus of claim 83 wherein at least one common control node of the field effect transistors are coupled in common, the two or more test circuits be accessible by applying appropriate signals to the first Vhigh signal, the second Vhigh signal and the Vlow signal of the respective test circuits.

85. The apparatus of claim 83 wherein the multiplexing circuit comprises complementary metal oxide semiconductor (CMOS) devices.

86. A test circuit comprising:

a pull up capacitive device having a first terminal, a control terminal and a common terminal;

a device under test coupled in series with the pull up capacitive device and having a common terminal coupled to the common terminal of the pull up capacitive device at a common node, a control terminal and a second terminal;

a voltage sense transistor having a drain, a gate coupled with the common node and a source; and

a duplicate transistor electrically substantially similar to the voltage sense transistor.

87. The test circuit of claim 86 wherein the pull up capacitive device substantially blocks all DC current and the device under test comprises a known-value capacitance with a leakage current to be characterized.

88. The test circuit of claim 87 wherein the device under test comprises a reverse-biased diode having a diode leakage current as the leakage current to be characterized.

89. The test circuit of claim 87 wherein the device under test comprises a tunnel oxide device having a tunneling current as the leakage current to be characterized.

90. The test circuit of claim 89 wherein the tunnel oxide device comprises a floating gate coupled to the common node.

91. The test circuit of claim 87 wherein the device under test comprises a tunnel oxide device having a hot electron programming current as the leakage current to be characterized.

92. The test circuit of claim 87 wherein the device under test comprises a tunnel oxide device having a hot carrier injection current through a gate oxide of the tunnel oxide device as the leakage current to be characterized.

93. The test circuit of claim 87 wherein the device under test comprises a metal oxide semiconductor (MOS) transistor having a hot carrier injection current through a gate oxide of the MOS transistor as the leakage current to be characterized.

94. The test circuit of claim 86 wherein the pull up capacitive device substantially blocks all DC current and the device under test comprises a capacitance that blocks substantially all DC current.

95. The test circuit of claim 86 wherein the voltage sense transistor is configured to receive a drain voltage and a source voltage and conduct drain current while the duplicate transistor receives the drain voltage and the source voltage and a variable gate voltage selected to match drain current of the duplicate transistor with drain current of the voltage sense transistor.

96. The test circuit of claim 89 further comprising:

a diode coupled to the common node to prevent over-charging of the common node.

97. A test circuit comprising:

a plurality of individual test circuits, each individual test circuit including a device under test and a voltage sense transistor, the voltage sense transistor having a source coupled to a common source probe pad;

one or more common signal sense nodes;

select transistors, a respective select transistor being coupled between a common signal sense node and respective individual test circuit; and

a duplicate transistor circuit including a duplicate voltage sense transistor and a duplicate select transistor, the duplicate voltage sense transistor having a source coupled to a duplicate sense source probe pad, a gate coupled to a duplicate sense gate probe pad, and a drain coupled in common with the drain of the duplicate select transistor, the duplicate select transistor having a source coupled to a duplicate select source probe pad and a gate coupled to a duplicate select gate probe pad.

98. The test circuit of claim 97 further comprising select gate bias probe pads, each select gate bias probe pad being in electrical communication with a gate of a respective select transistor and configured to receive a select bias signal.

99. The test circuit of claim 97 wherein the respective individual test circuit comprises:

a pull up capacitive device having a common terminal and a control terminal, the common terminal being coupled to the gate of the voltage sense transistor, the control terminal being coupled in common with a probe pad and with the control terminals of other individual test circuits of the test circuit;

a device under test coupled with the pull up capacitive device and having a common terminal coupled in common with the common terminal of the pull up capacitive device at a common node, and a control terminal, the control terminal being coupled to a probe pad in common with the control terminals of other individual test circuits of the test circuit.

100. The test circuit of claim 99 wherein the device under test comprises a reverse biased diode, respective individual test circuits including a respective reverse biased diode varying from other respective reversed biased diodes by some feature.

101. The test circuit of claim 100 wherein the feature comprises one or more of the dimensions of the diode.

102. The test circuit of claim 99 wherein the common signal sense node comprises a common probe pad configured to receive a drain bias voltage and a drain current for a plurality of devices under test.

103. The test circuit of claim 102 further comprising:

an n-well bias voltage probe pad; and

a substrate bias probe pad.

104. The test circuit of claim 97 wherein the respective individual test circuit comprises:

a pull up capacitive device having a common terminal and a control terminal, the common terminal being coupled to the gate of the voltage sense transistor, the control terminal being coupled in common with a probe pad and with the control terminals of other individual test circuits of the test circuit;

a pull down capacitive device having a common terminal coupled in common with the common terminal of the pull up capacitive device at a common node, a control terminal coupled in common with a probe pad and in common with the control terminals of other individual test circuits of the test circuit;

a device under test coupled with the pull up capacitive device and with the pull down capacitive device and having a common terminal coupled in common with the common terminal of the pull up capacitive device and with the common terminal of the pull down capacitive device at a common node, and a control terminal coupled to a probe pad in common with the control terminals of other individual test circuits of the test circuit.

105. The test circuit of claim 104 wherein the device under test comprises a reverse biased diode, respective individual test circuits including a respective reverse biased diode varying from other respective reversed biased diodes by some feature.

106. The test circuit of claim 105 wherein the feature comprises one or more of the dimensions of the diode.

107. The test circuit of claim 104 wherein the common signal sense node comprises a common probe pad configured to receive a drain bias voltage and a drain current for a plurality of devices under test.

108. The test circuit of claim 107 further comprising:

an n-well bias voltage probe pad; and

a substrate bias probe pad.